MULTI-LAYER CIRCUIT BOARD

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a multi-layer circuit board, more particularly to a multi-layer circuit board which can achieve impedance matching to result in reduced high speed signal reflection and reduced electromagnetic interference.

2. Description of the Related Art

According to industrial standards, multi-layer circuit boards with eight wiring layers generally include the 1.2 mm type and the 1.6 mm type. Figure 1 shows a conventional multi-layer circuit board with a thickness of about 1.2 mm, which includes: first, second, third, fourth, fifth, sixth and seventh insulating substrates (A1), (A2), (A3), (A4), (A5), (A6), (A7) disposed sequentially one above the other; a first signal wiring layer (S1) disposed on one side of the first insulating substrate (A1) opposite to the second insulating substrate (A2); a first ground wiring layer (GND1) disposed between the first and second insulating substrates (A1), (A2); a second signal wiring layer (S2) disposed between the second and third insulating substrates (A2), (A3); a third signal wiring layer (S3) disposed between the third and fourth insulating substrates (A3), (A4); a power wiring layer (POWER) disposed between the fourth and fifth

insulating substrates (A4), (A5); a fourth signal wiring layer (S4) disposed between the fifth and sixth insulating substrates (A5), (A6); a second ground wiring layer (GND2) disposed between the sixth and seventh insulating substrates (A6), (A7); and a fifth signal wiring layer (S5) disposed on one side of the seventh insulating substrate (A7) opposite to the sixth insulating substrate (A6). Each of the first, third, fifth and seventh insulating substrates (A1), (A3), (A5), (A7) is made from a polyester prepreg. Each of the second, fourth and sixth insulating substrates (A2), (A4), (A6) is made from a fibrous core material that contains paper or glass fibers.

In addition, each of the first and seventh insulating substrates (A1), (A7) has a thickness (H4) of about 2.5 mil. Each of the second and sixth insulating substrates (A2), (A6) has a thickness (H3) of about 8 mil. Each of the third and fifth insulating substrates (A3), (A5) has a thickness (H2) of about 5 mil. The fourth insulating substrate (A4) has a thickness (H1) of about 8 mil. The first signal wiring layer (S1) has a first resistance (Rs1) with respect to the first ground wiring layer (GND1). The second signal wiring layer (S2) has a second resistance (Rs2) with respect to the first ground wiring layer (GND1) and the power wiring layer (POWER). The third signal wiring layer (S3) has a third resistance (Rs3) with

respect to the first ground wiring layer (GND1) and the power wiring layer (POWER). The fourth signal wiring layer (S4) has a fourth resistance (Rs4) with respect to the second ground wiring layer (GND2) and the power wiring layer (POWER). The fifth signal wiring layer (S5) has a fifth resistance (Rs5) with respect to the second ground wiring layer (GND2). The first and fifth resistances (Rs1), (Rs5) are about 44 ohms. The second, third and fourth resistances (Rs2), (Rs3), (Rs4) are about 51 ohms.

Figure 2 shows a conventional multi-layer circuit board having a thickness of about 1.6 mm. The 1.6 mm circuit board differs from the above-described 1.2 mm circuit board in that H4 is equal to 9.5 mil, instead of 2.5 mil. Hence, the first and fifth resistances (Rs1), (Rs5) are about 76.4 ohms.

Due to their construction, the conventional multi-layer circuit boards shown in Figures 1 and 2 have the following disadvantages:

1. Serious high speed signal reflection

According to the standard theoretical values determined by Intel, the resistance between two adjacent wiring layers for a circuit board during high speed signal transmission is preferably within the range of $55 \pm 10\% \Omega$, i.e., between 49.5Ω and 60.5Ω. However, the first and fifth resistances (Rs1), (Rs5), being about 44 ohms, of the aforementioned conventional

1.2 mm circuit board fall outside the preferred range recommended by Intel, and there is additionally a difference of 7 ohms between the value of the first and fifth resistances (Rs1), (Rs5) and that of the second, third and fourth resistances (Rs2), (Rs3), (Rs4). Such a difference will result in an impedance mismatch. Thus, when a high speed signal is being transmitted through the conventional 1.2 mm circuit board and passes from the first or fifth wiring layer (S1) or (S5) to the second, third or fourth wiring layer (S2) or (S3) or (S4), reflection of the signal will result, thereby adversely affecting signal transmission. Likewise, the value of the first and fifth resistances (Rs1), (Rs5) of the aforementioned conventional 1.6 mm circuit board falls outside the theoretical range, and there is a large difference present between the value of the first and fifth resistances (Rs1), (Rs5) and that of the second, third and fourth resistances (Rs2), (Rs3), (Rs4). The reflection index of high-speed signals for the 1.2 mm circuit board can be calculated as follows:

$$\rho = \frac{Zl - Zo}{Zl + Zo} = \frac{Rs1 - Rs2}{Rs1 + Rs2} = 0.07$$

The reflection index for the 1.6 mm circuit board can be calculated in a similar manner and is found to be even higher, being 0.2. The signal reflection is therefore very serious, which results in considerable distortion of the waveform and poor signal quality.

(2) Weakened magnetic flux counteraction: As reflection of high speed signals will generate standing waves, which will increase electromagnetic radiation of the high speed signals, the magnetic flux counteraction of the circuit board is weakened, thereby resulting in excessively high electromagnetic interference.

SUMMARY OF THE INVENTION

Therefore, the main object of the present invention is to provide a multi-layer circuit board which can achieve impedance matching to result in reduced high speed signal reflection and reduced electromagnetic interference.

Accordingly, a multi-layer circuit board according to the present invention includes: first, second, third, fourth, fifth, sixth and seventh insulating substrates disposed sequentially one above the other; a first signal wiring layer disposed on one side of the first insulating substrate opposite to the second insulating substrate; a first ground wiring layer disposed between the first and second insulating substrates; a second signal wiring layer disposed between the second and third insulating substrates; a third signal wiring layer disposed between the third and fourth insulating substrates; a power wiring layer disposed between the fourth and fifth insulating substrates; a fourth signal wiring layer disposed between the fifth and sixth

insulating substrates; a second ground wiring layer disposed between the sixth and seventh insulating substrates; and a fifth signal wiring layer disposed on one side of the seventh insulating substrate opposite to the sixth insulating substrate. Each of the first and seventh insulating substrates has a thickness ranging from 2.5 to 6.5 mil. Each of the second, fourth and sixth insulating substrates has a thickness ranging from 3 to 9 mil. Each of the third and fifth insulating substrates has a thickness ranging from 3 to 23 mil. The first signal wiring layer has a first resistance with respect to the first ground wiring layer. The second signal wiring layer has a second resistance with respect to the first ground wiring layer and the power wiring layer. The third signal wiring layer has a third resistance with respect to the first ground wiring layer and the power wiring layer. The fourth signal wiring layer has a fourth resistance with respect to the second ground wiring layer and the power wiring layer. The fifth signal wiring layer has a fifth resistance with respect to the second ground wiring layer. The first, second, third, fourth and fifth resistances are within the range of 49.5 to 60.5 ohms.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the present invention will become apparent in the following

detailed description of the preferred embodiments with reference to the accompanying drawings, of which:

Figure 1 is a schematic view of a conventional multi-layer circuit board with a thickness of about 1.2 mm;

Figure 2 is a schematic view of another conventional multi-layer circuit board with a thickness of about 1.6 mm;

Figure 3 is a schematic view of the first preferred embodiment of a multi-layer circuit board with a thickness of about 1.2 mm according to the present invention;

Figure 4 is a sectional view of the first preferred embodiment in part;

Figure 5 is another sectional view of the first preferred embodiment in part; and

Figure 6 is a schematic view of the second preferred embodiment of a multi-layer circuit board with a thickness of about 1.6 mm according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before the present invention is described in greater detail, it should be noted that like elements are denoted by the same reference numerals throughout the disclosure.

Referring to Figures 3 to 5, the first preferred embodiment of a multi-layer circuit board 2 with a

thickness of about 1.2 mm according to the present invention is shown to include: first, second, third, fourth, fifth, sixth and seventh insulating substrates (B1), (B2), (B3), (B4), (B5), (B6), (B7) disposed sequentially one above the other; a first signal wiring layer (S1) disposed on one side of the first insulating substrate (B1) opposite to the second insulating substrate (B2); a first ground wiring layer (GND1) disposed between the first and second insulating substrates (B1), (B2); a second signal wiring layer (S2) disposed between the second and third insulating substrates (B2), (B3); a third signal wiring layer (S3) disposed between the third and fourth insulating substrates (B3), (B4); a power wiring layer (POWER) disposed between the fourth and fifth insulating substrates (B4), (B5); a fourth signal wiring layer (S4) disposed between the fifth and sixth insulating substrates (B5), (B6); a second ground wiring layer (GND2) disposed between the sixth and seventh insulating substrates (B6), (B7); and a fifth signal wiring layer (S5) disposed on one side of the seventh insulating substrate (B7) opposite to the sixth insulating substrate (B6). The first, second, third, fourth and fifth signal wiring layers (S1), (S2), (S3), (S4), (S5) are generally made from copper coil. The first and fifth signal wiring layers (S1), (S5) are adapted to be mounted with electronic components (not

shown) thereon. At least one of the first, third, fifth and seventh insulating substrates (B1), (B3), (B5), (B7) is made from a polyester prepreg. At least one of the second, fourth and sixth insulating substrates (B2), (B4), (B6) is made from a fibrous core material which contains paper or glass fibers.

According to the present invention, each of the first and seventh insulating substrates (B1), (B7) has a thickness (H4) ranging from 2.5 to 6.5 mil. Each of the second and sixth insulating substrates (B2), (B6) has a thickness (H3) ranging from 3 to 9 mil. Each of the third and fifth insulating substrates (B3), (5) has a thickness (H2) ranging from 3 to 23 mil. The fourth insulating substrate (B4) has a thickness (H1) ranging from 3 to 9 mil. Preferably, the thicknesses (H4) of the first and seventh insulating substrates (B1), (B7) are equal. The thicknesses (H3) of the second and sixth insulating substrates (B2), (B6) are equal. The thicknesses (H2) of the third and fifth insulating substrates (B3), (B5) are equal.

The first, second, third, fourth, fifth, sixth and seventh insulating substrates (B1), (B2), (B3), (B4), (B5), (B6), (B7), the first, second, third, fourth and fifth signal wiring layers (S1), (S2), (S3), (S4), (S5), the first and second ground wiring layers (GND1), (GND2), and the power wiring layer (POWER) are press-bonded to each other to form the circuit board

2 with a thickness of about 1.2 mm. During press-bonding of the circuit board 2, the third signal wiring layer (S3) and the power wiring layer (POWER) are disposed to sandwich the fourth insulating substrate (B4). Then, the second signal wiring layer (S2) and the third signal wiring layer (S3), and the fourth signal wiring layer (S4) and the power wiring layer (POWER) are disposed to sandwich the third and fifth insulating substrates (B3), (B5), respectively. The first ground wiring layer (GND1) and the second signal wiring layer (S2), and the fourth signal wiring layer (S4) and second ground wiring layer (GND2) are disposed to sandwich the second and sixth insulating substrates (B2), (B6). Finally, the first signal wiring layer (S1) and the first ground wiring layer (GND1), and the fifth signal wiring layer (S5) and the second ground wiring layer (GND2) are disposed to sandwich the first and seventh insulating substrates (B1), (B7) to constitute the 1.2 mm multi-layer circuit board 2.

According to the first preferred embodiment, each of the first and fifth signal wiring layers (S1), (S5) has a thickness of about 1.4 mil. Each of the second, third and fourth signal wiring layers (S2), (S3), (S4), the first and second ground wiring layers (GND1), (GND2), and the power wiring layer (POWER) has a thickness of about 0.7 mil. In addition, each of the third and fifth insulating substrates (B3), (B5) has

a preferred thickness (H2) ranging from 3 to 9 mil, more preferably 6 mil. Each of the first and seventh insulating substrates (B1), (B7) has a preferred thickness (H4) of 4.5 mil. Each of the second, fourth, and sixth insulating substrates (B2), (B4), (B6) has a preferred thickness (H3, H1) of 6 mil. The first signal wiring layer (S1) has a first resistance (Rs1) with respect to the first ground wiring layer (GND1). The second signal wiring layer (S2) has a second resistance (Rs2) with respect to the first ground wiring layer (GND1) and the power wiring layer (POWER). The third signal wiring layer (S3) has a third resistance (Rs3) with respect to the first ground wiring layer (GND1) and the power wiring layer (POWER). The fourth signal wiring layer (S4) has a fourth resistance (Rs4) with respect to the second ground wiring layer (GND2) and the power wiring layer (POWER). The fifth signal wiring layer (S5) has a fifth resistance (Rs5) with respect to the second ground wiring layer (Rs2). With the thicknesses of the insulating substrates (B1), (B2), (B3), (B4), (B5), (B6), (B7) controlled to be within the aforementioned ranges, the first, second, third, fourth and fifth resistances (Rs1), (Rs2), (Rs3), (Rs4), (Rs5) can be kept within the range of 49.5 to 60.5 ohms to thereby achieve impedance matching.

The calculation of the approximate thickness of each of the insulating substrates (B1), (B2), (B3), (B4),

(B5), (B6) and (B7) is explained in the following description.

Firstly, the value of the first and fifth resistances (Rs1), (Rs5) is calculated using the following Formula (1):

$$Rs1=Rs5=\frac{87}{\sqrt{E_R+1.41}}\ln\left\{\frac{5.98H4}{0.8W+T1}\right\}\ldots\ldots1$$

wherein E_R is the dielectric coefficient and is equal to 4.5; H4 is the thickness of the first and seventh insulating substrates (B1), (B7); W is the width of traces of the first and fifth signal wiring layers (S1), (S5) and is within the range of 2 to 8 mil and is equal to 5 mil in this preferred embodiment; and T1 is the thickness of the first and fourth signal wiring layer (S1), (S4) and is equal to 1.4 mil.

Next, the value of the second and third resistances (Rs2), (Rs3) is obtained using the following Formulae (2) and (3):

$$Rs2=Rs3=\frac{2YZ}{Y+Z}\}\ldots\ldots2$$

$$Y=\frac{60}{\sqrt{ER}}\ln\left\{\frac{8H3}{0.67\pi W\left(0.8+\frac{T2}{W}\right)}\right\}$$

$$Z=\frac{60}{\sqrt{ER}}\ln\left\{\frac{8(H3+H2)}{0.67\pi W\left(0.8+\frac{T2}{W}\right)}\right\}\quad\ldots\ldots 3$$

wherein E_R is the dielectric coefficient and is equal to 4.5; H3 is the thickness of the second and sixth insulating substrates (B2), (B6) and is equal to H1, the thickness of the fourth insulating substrate (B4); H2 is the thickness of the third and fifth insulating substrates (B3), (B5); T2 is the thickness of the second signal wiring layer (S2) and is equal to 0.7 mil, which is also the thickness of the third signal wiring layer (S3); and W is the width of traces of the second and third signal wiring layers (S2), (S3) and is within the range of 2 to 8 mil. In this preferred embodiment, W is equal to 5 mil.

The value of the fourth resistance (Rs4) is obtained using the following Formula (4):

$$Rs4=\frac{60}{\sqrt{ER}}\ln\left\{\frac{4(H2+H3)}{0.67\pi W\left(0.8+\frac{T2}{W}\right)}\right\}\quad\ldots\ldots 4$$

wherein E_R is the dielectric coefficient and is equal to 4.5; H3 is the thickness of the second and sixth insulating substrates (B2), (B6); H2 is the thickness of the third and fifth insulating substrates (B3), (B5); T2 is the thickness of the fourth signal wiring layer (S4) and is equal to 0.7 mil; and W is the width of traces

of the fourth signal wiring layer (S4) and is within the range of 2 to 8 mil. In this preferred embodiment, W is equal to 5 mil.

$$2H4+2H3+2H2+1H1+2T1+6T2\cong 48 \text{ mil}.....5$$

In addition, the total thickness of the circuit board should be equal to 1.2 mm (equivalent to about 48 mil) or within a tolerance range thereof, as expressed by the Formula (5). Based on the above Formula (5), the preferred value of thickness of each of the insulating substrates can be obtained. That is, when H1, the thickness of the fourth insulating substrate (B4) is within the range of 3 to 9 mil, H1 is preferably equal to 6 mil. When H2, the thickness of the third and fifth insulating substrates (B3), (B5) is within the range of 3 to 9 mil, H2 is preferably equal to 6 mil. When H3, the thickness of the second and sixth insulating substrates (B2), (B6) is within the range of 3 to 9 mil, H3 is preferably equal to 6 mil. When H4, the thickness of the first and seventh insulating substrates (B1), (B7) is within the range of 2.5 to 6.5 mil, H4 is preferably equal to 4.5 mil. Under this condition, the first and fifth resistances (Rs1), (Rs5) are about 58 ohms. The second and third resistances (Rs2), (Rs3) are about 57 ohms. The fourth resistance (Rs4) is about 50 ohms. All of these resistance values fall within the theoretical range of 49.5 to 60.5 ohms recommended by Intel for high speed signal transmission.

Besides, the total thickness of the circuit board 2 fulfills the Formula (5) in which 2H4+2H3+2H2+1H1+2T1+6T2=2X4.5mil+2X6 mil+2X6 mil+1X6 mil+2X1.4mil+6X0.7mil=46mil≒1.2 mm (within tolerance range).

Figure 6 shows the second preferred embodiment of a multi-layer circuit board 2' according to the present invention. The circuit board 2' is shown to include first, second, third, fourth, fifth, sixth and seventh insulating substrates (B1'), (B2'), (B3'), (B4'), (B5'), (B6'), (B7'), first, second, third, fourth and fifth signal wiring layers (S1), (S2), (S3), (S4), (S5), first and second ground wiring layers (GND1), (GND2), and a power wiring layer (POWER), all of which are press-bonded to each other to form the circuit board 2' with a thickness of about 1.6 mm. This preferred embodiment differs from the previous embodiment in that each of third and fifth insulating substrates (B3'), (B5') has a thickness (H2) ranging from 9 to 23 mil. After a calculation based on the above formulae, the following preferred values for H1, H2, H3 and H4 are obtained. H1 is preferably within the range of 3 to 9 mil, and is more preferably equal to 6 mil. H2 is preferably within the range of 9 to 23 mil, and is more preferably equal to 16 mil. H3 is preferably within the range of 3 to 9 mil, and is more preferably equal to 6 mil. H4 is preferably within the range of 2.5 to

6.5 mil, and is more preferably equal to 4.5 mil. As such, the first and fifth resistances are about 60 ohms. The second and third resistances are about 55 ohms. The fourth resistance is about 60 ohms. All of these resistance values fall within the theoretical range recommended by Intel.

Accordingly, the multi-layer circuit board of the present invention has the following advantages:

1. Reduced high speed signal reflection

Since the resistances in both of the first and second preferred embodiments all fall within the recommended range of $55\Omega \pm 10\%$, the reflection indexes are substantially low as compared to those in the prior art. Therefore, reflection of high speed signals can be significantly reduced to make the circuit board highly suitable for high speed signal transmission.

2. Reduced electromagnetic interference

As a result of reduced high speed signal reflection, generation of standing waves is not likely. Hence, magnetic flux counteraction can be enhanced to reduce electromagnetic interference to meet current EMI standards.

3. Better adaptability for high speed signal layout

In view of the aforementioned advantages, the circuit board of this invention is suited for high speed signal layout to meet the current trend in the industry toward high speed signal development and to enhance

market value of products and market competitiveness.

4. Enhanced layout time efficiency

Due to impedance matching, there is no need to alter the width of traces of the signal wiring layers, thereby improving the layout time efficiency.

While the present invention has been described in connection with what is considered the most practical and preferred embodiments, it is understood that this invention is not limited to the disclosed embodiments but is intended to cover various arrangements included within the spirit and scope of the broadest interpretation so as to encompass all such modifications and equivalent arrangements.